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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/822,166	03/30/2001	Ritesh Saraf	03226.082001;P5751	6279

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ROSENTHAL & OSHA L.L.P. / SUN  
1221 MCKINNEY, SUITE 2800  
HOUSTON, TX 77010

EXAMINER

DOOLEY, MATTHEW C

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 12/23/2003

4

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/822,166

Applicant(s)

SARAF, RITESH

Examiner

Matthew C. Dooley

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 March 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 March 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

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## DETAILED ACTION

### *Drawings*

1. The informal drawings are of sufficient quality for examination purposes. However, new formal drawings will be required if and when the application is put in condition for allowance.

### *Claim Objections*

2. Claim 3 is objected to because of the following informalities: Claim 3 includes language "resides on another end of the flip-flop circuit". The language seems to suggest placement of the scan input control stage in relation to the data input control stage. However, claim 3 does not include reference to claim 2 where the location of the data input control stage is referenced. This problem can be corrected by changing the dependency of claim 3 to depend from claim 2 or by including language that identifies more clearly what circuitry exists in relation to the scan input control stage. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsunaga et al., U.S. 6,150,861.

As per claim 1:

Matsunaga teaches to flip-flop (f-f) circuitry that includes a data input control stage that selectively controls a value on a data node that is coupled to the master stage and the slave stage and a scan input control stage that selectively controls a value on a scan node that is coupled to the master stage (Fig.2).

As per claim 2:

Matsunaga teaches to f-f circuitry wherein the data input control stage inputs a data input signal and a scan enable signal, and wherein the data input control stage resides on the topmost end of the f-f circuit (Fig.1,2).

As per claim 3:

Matsunaga teaches to f-f circuitry wherein the scan input control stage inputs a scan input signal and a scan enable signal, wherein the scan input control stage resides on the bottommost end of the f-f circuit (Fig.1,2).

As per claim 4:

Matsunaga teaches to circuitry that pulls the data node to a first value when the f-f is in a scan mode (Fig.2; Col.2: 33-67).

As per claim 5:

Matsunaga teaches to a scan node that is active during the scan mode (Col.2: 35-36).

As per claim 6:

Matsunaga teaches to the scan node being pulled to a second value when the f-f is in normal mode, and wherein the data node is active during normal mode (Col.2: 33-42).

As per claim 7:

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Matsunaga teaches to the master stage passing a value to the slave stage based on the scan and data node values (Fig.2; Col.3: 15-16).

As per claim 8:

Matsunaga teaches to delayed and inverted clock signals to the data and scan input control stages and the master and slave stages (Fig.1, 2; Col. 3: 30-45).

As per claim 9:

Matsunaga teaches to a data input signal that selectively controls the value on the data node dependent on the clock input control stage (Col.3: 30-54).

As per claim 10:

Matsunaga teaches to a data input signal that selectively controls the value on the scan node dependent on the clock input control stage (Col.3: 30-54).

As per claim 11:

Matsunaga teaches to the master stage selectively passing a value to the slave stage dependent on the data and scan nodes and the clock input control stage (Fig.2: Col.3: 30-54).

As per claim 12:

Matsunaga teaches to the slave stage selectively controlling the output value of the f-f dependent on the data node and the clock input control stage (Fig.2: Col.3: 30-54).

As per claim 13:

Matsunaga teaches to f-f methodology that includes selectively controlling a value on a data node dependent on a data input control stage and the clock input control stage, wherein the data node is coupled to the master and slave stage, selectively controlling a

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value on a scan node dependent on a scan input control stage and the clock input control stage, wherein the scan node is coupled to the master stage, selectively controlling the slave stage dependent on the master stage and the clock input control stage, and selectively generating an output of the f-f dependent on the slave stage (Fig. 1, 2; Col.2: 33-67; Col.3: 30-54).

As per claim 14:

Matsunaga teaches to holding the data node to a first value when the f-f is in a scan mode (Fig.2; Col.2: 33-67).

As per claim 15:

Matsunaga teaches to a scan node that is active during the scan mode (Col.2: 35-36).

As per claim 16:

Matsunaga teaches to holding the scan node being pulled to a second value when the f-f is in normal mode (Col.2: 33-42).

As per claim 17:

Matsunaga teaches to the data node being active during normal mode (Col.2: 33-42).

As per claim 18:

Matsunaga teaches inputting a clock signal to the clock input control stage and generating delayed and inverted clock signals (Fig.1, 2; Col. 3: 30-45).

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***Conclusion***


5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

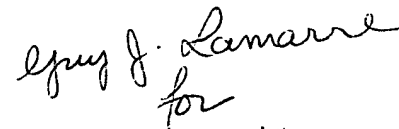
- |    |                 |                           |
|----|-----------------|---------------------------|
| a. | Gregor et al.   | U.S. 5,920,575: Fig. 4    |
| b. | Kakizawa et al. | U.S. 2002/0112208: Fig. 1 |

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Dooley whose telephone number is (703) 306-5538. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

  
Matthew Dooley  
Examiner Au 2133  
12/12/03

  
for  
Albert DeCady  
Primary Examiner